Amendments to the Specification

Please amend the paragraph beginning on line 16 of page 1 as follows:

Eye diagrams are usually generated to determine the modulation characteristics of received data signals. The shape of an eye diagram changes depending on a number of receiver-related factors including noise margin, tolerances for timing and amplitude variations, and others generally ~~Generally~~, the width of the eye determines the timing margin and the widths of the eye transition points determine jitter. Also, a direct correlation exists between eye shape and the type of logic used to construct the receiver circuits. For example, current mode logic has a tendency to produce an irregularly shaped eye, whereas other logic types produce eyes with greater symmetry.

Please amend the paragraph beginning on line 7 of page 8 as follows:

Fig. 2 shows an example of how the interpolators may be implemented to generate phase signals from differential in-phase and quadrature inputs. The I phase interpolator is shown as receiving differential $I^{\pm}$ ~~I"~~ and $Q^{\pm}$ ~~Q"~~ signals from which the I signal phase RI is generated based on control information IP_i generated from controller 4. The Q phase interpolator is shown as receiving the same differential $I^{\pm}$ ~~I"~~ and $Q^{\pm}$ ~~Q"~~ signals from which the Q signal phase RQ is generated based on control information QP_i generated from controller 4. In accordance with the present embodiment, the value of QP_i is independently adjusted to cause the RQ phase to match a predetermined point on the eye diagram, which is preferably the ideal sampling point. An example of this circuit is discussed in greater detail below, where the control information into the interpolators are provided as 32-bit information.

Please amend the paragraph beginning on line 7 of page 9 as follows:

An initial block includes receiving a data signal to be sampled. (Block 100). The data signal may be one transmitted in a high-speed signaling system, a communication system, or any other system designed to transmit, receive, or otherwise carry data signals. The signals may be optical signals including but not limited to those in a synchronous optical network

(SONET), wireless signals which conform to any one of a number of communications standards (e.g., CDMA, GSM, IMT-2000), as well as wireline signals.

Please amend the paragraph beginning on line 1 of page 10 as follows:

Next, the phases of the in-phase and quadrature signals are determined. (Block 140). Fig. 4 shows an example of how differential forms of the in-phase and quadrature signals may be plotted on a four-phase clock diagram. In this diagram, differential in-phase components are referenced along the horizontal axis and differential quadrature phase components are referenced along the vertical axis. The phases of the differential in-phase and quadrature signals RI^+, RI^-, RQ^+, and RQ^- as demodulated are shown for illustrative purposes as residing along the axes. (Because the demodulation is performed using, for example, 90 degree-shifted versions of a local oscillator, $\underline{RI^{\pm}}$ ~~$RI^{''}$~~ are orthogonal to $\underline{RQ^{\pm}}$ ~~$RQ^{''}$~~ respectively. Also, RI^+ and RI^- differ in phase by $\underline{180°}$ ~~180E~~ and the same is true for RQ^+ and RQ^-.)

Please amend the paragraph beginning on line 14 of page 11 as follows:

Fig. 7 shows a mapping of the phase signals onto the eye diagram after the first shift. The shifted phase RI^+ now coincides with crossing point X and the same is true of RI^- with respect to a succeeding crossing point. Consecutive phases are still separated by $\underline{90°}$ ~~90E~~. If after the first phase shift, the quadrature signal phase RQ^+ does not coincide with ideal sampling point C, then even though the in-phase differential signals are mapped to the crossing points an optimum BER will not be realized during sampling. To optimize BER, a second phase shift may then be performed.

Please amend the paragraph beginning on line 14 of page 14 as follows:

After the in-phase and quadrature signal phases are shifted to predetermined positions, at least one of these signals is input as a clock signal for controlling the data sampler. (Block 180). Preferably, the differential forms of the quadrature phase signal is

used for this purpose, however the in-phase signal may alternatively be used. The sampler samples the received data signal based on the timing information in the clock signal. This is accomplished by sampling the data signal with all four clock phases. All four sampled data bits (DRI+, DRQ+, DRI-, DRQ- ~~DRI-~~) are then synchronized to one clock domain to allow digital processing of the edge detection circuitry.

Please amend the paragraph beginning on line 14 of page 27 as follows:

Fig. 15 shows a system which includes a processor 300 and a memory 410 ~~310~~. The processor may include an internal arithmetic logic unit 302 and cache 304, and the memory may be a random access memory or any other type of memory capable of storing data generated, processed, or otherwise controlled by or transferred through the processor. The processor and preferably the memory receive power from supply 420 ~~320~~. The system may also include an external memory (e.g., cache) 380 ~~330~~, a chipset 440 ~~340~~, a graphical interface 450 ~~350~~, and a network interface 460 ~~360~~. These features are considered to be optional in the system.